HiSilicon Achieves PPA Targets Quicker Using PrimeTime POCV to Reduce Design Margin on TSMC N7 FinFET Process

Synopsys / HiSilicon

ABSTRACT

Join this session to learn about HiSilicon's latest tapeout experience on TSMC N7 FinFET process and how Synopsys' PrimeTime POCV technology delivered signoff accuracy with reduced pessimism at low voltages.

This session covers the unique characteristic of TSMC advanced FinFET transistors that not only can reach 3Ghz+ frequency at normal voltages, but also achieve ultra-low power consumption at voltages down to 0.45V, albeit with a longer cell delay and broader timing variation.

Traditional margining methodologies applies a global derate that can result in significant timing pessimism, especially at low voltages to be timing safe, introducing challenges to meet PPA targets and signoff timing.

HiSilicon and Synopsys will share the innovations in PrimeTime POCV that overcome this over margining challenge by modeling cell delay and output slew with statistical mean and sigma based on input slew and output load using TSMC LVF libraries. This level of granularity not only accurately captures the critical timing paths, but also removes unnecessary pessimism by statistical cancellation to accelerate signoff timing closure and achieve PPA targets quicker.

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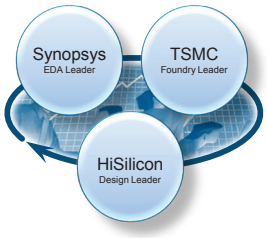
Agenda

- Synopsys PrimeTime POCV Technology
- HiSilicon Experience with PrimeTime POCV

3-way Collaboration Highlights

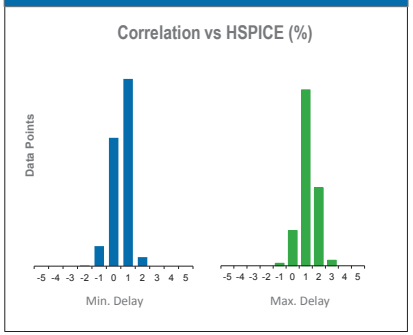
- **Tight collaboration between TSMC, HiSilicon, and Synopsys enables first-to-market advanced chips**
  - 1st TSMC N16FF production chip
  - Early design start TSMC N10FF production
  - Early design start TSMC N7FF production
  - and more to come…



Superior FinFET Signoff Accuracy

PrimeTime is most trusted signoff tool for FinFET designs

PrimeTime N7FF 0.45V Delay Accuracy



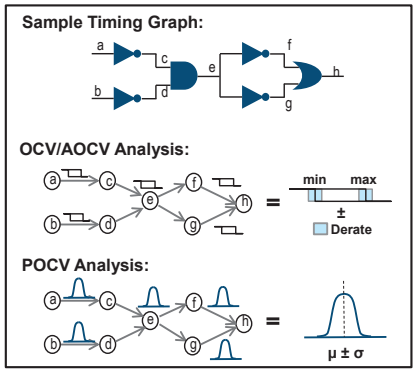
- 90% of the leading volume-production SoCs have been designed with the Galaxy Flow
- **Top customers selecting PrimeTime as signoff PoR for N7 FinFET Designs**

Low Voltage Golden Accuracy using Advanced Waveform Propagation

Source: Synopsys Internal Testing

Evolution of Variation Analysis and Signoff

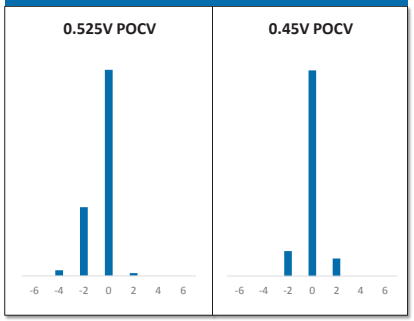
- **OCV applies additional derate on min/max corners based on lib cell**
  - Single derate for all cell instances
- **AOCV can apply derate based on cell type and stage**
  - GBA pessimism pose impact to PPA
- **POCV models timing as true statistical distributions**
  - Delay/Transition/Constraint variation modeling
  - Consistent variation modeling in implementation & signoff



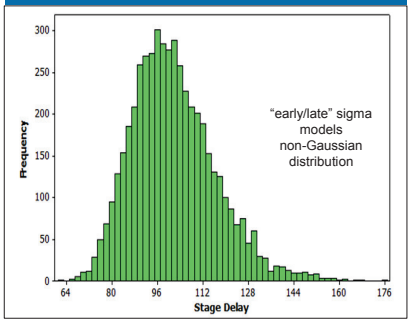
POCV Tapeout Proven for Low Voltage

50+ FinFET tapouts with PrimeTime POCV

PrimeTime N7FF Variation Accuracy Vs HSPICE Monte-Carlo

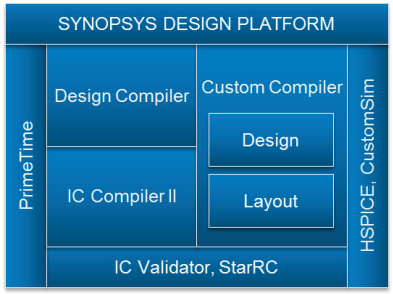


POCV Asymmetrical Distribution Modeling



Source: Synopsys Internal Testing

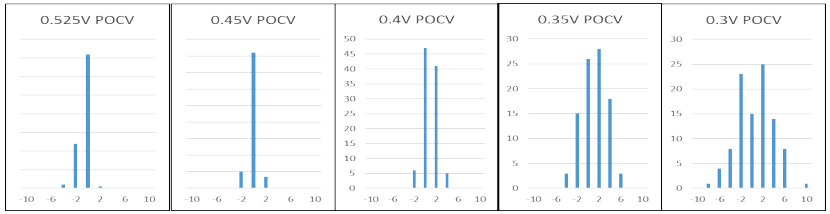
Galaxy Design Platform is POCV-Ready



Function (Tools)	POCV Readiness
Characterization (SiliconSmart)	✓
Library Prep. (Library Compiler)	✓
Synthesis (Design Compiler)	✓
Place & Route (IC Compiler II)	✓
Signoff (PrimeTime)	✓
Transistor STA (NanoTime)	✓

Future: Impact of Ultra-Low Power Methodologies

- **Variation increases drastically with Ultra-low Voltage**
  - TSMC and Synopsys have closely collaborated and extensions of LVF are available today



Source: Synopsys Internal Testing

Today's common voltage range → Preparation for future

Agenda

Synopsys PrimeTime POCV Technology

➡ HiSilicon Experience with PrimeTime POCV

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HiSilicon Mobile Design Leadership - Kirin

- **Industry 1st FinFET Mobile Design**
  - Built on TSMC N16FF in 2014
  - Latest model in production on TSMC N7
- **Includes high performance CPU cluster**
  - Dynamic scaling for mobile power requirement
  - Target 3Ghz+ @ 0.7V ± 10%
  - Target 500Mhz @ 0.5V ± 10%; 5mw or below
- **Low voltage accuracy is main focus for timing closure and signoff**
  - Larger delay and variability at low voltages
  - Traditional margining may be too pessimistic

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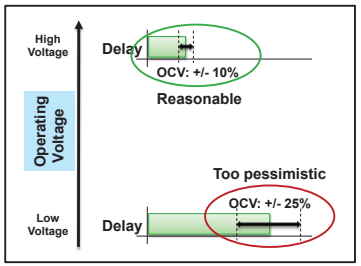
Challenge of Variation Modeling of Low Voltage N7FF

- **TSMC N7 FinFET transistors can operate at wide voltage ranges**
  - More frequency and voltage modes achievable (DVFS); especially important for mobile
- **High-speed transistors operating at low voltages exhibit wider variation**
  - Variation at high voltages are same as before
  - Increased margins required at low voltage
- **Techniques need to evolve to model variation accurately and efficiently**
  - Apply larger OCV only where needed



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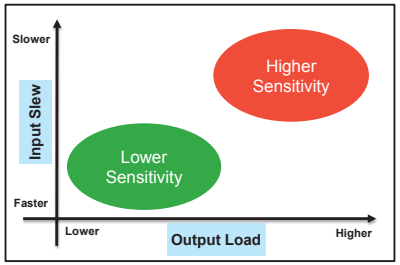
Modeling Slew and Load Dependent Variability

- **Larger variation at low voltages requires additional OCV margining**
  - Larger variation caused by higher cell sensitivity to process variation
- **Cells with slower slew and/or higher load is more sensitive to process variation**
  - Only such cells require larger margining
- **Variation modeling technique for low voltage designs need to be slew/load dependent**
  - Avoid pessimism/optimism caused by single global derate margin



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POCV Benefit – Low Voltage Evaluation Data

- **PPA Comparison at Lowest Voltage Corner (0.5V ± 10%)**
  - Design: High performance CPU core for mobile application
  - Library: TSMC N7FF LVF library with early/late sigma
- **Evaluation: POCV delay/slew and constraint variation enabled**
  - Reference: OCV global derate for low voltage corner

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HiSilicon Selects PrimeTime POCV for Low Voltage Signoff

- **TSMC FinFET transistors enable wide range for dynamic voltage/frequency scaling**
  - Important for HiSilicon leading edge mobile designs built on TSMC N7FF process
- **At low voltages, larger variation requires additional OCV margining**
  - Larger margining only need to be applied to cells with slow slew and/or large load
  - Global margining will be too pessimistic and impact timing closure and signoff
- **TSMC N7FF LVF libraries and POCV accurately models slew/load dependent variation**
  - Reduces over margining and maintaining signoff accuracy
  - Achieve best PPA without unnecessary over designing and redundant cycles
- **Additional POCV advantage at FinFET is availability throughout implementation flow**
  - Tighten the gap between graph-based and path-based analysis for better implementation QoR
  - Future proof with support ready for moment-based extensions

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Thank You